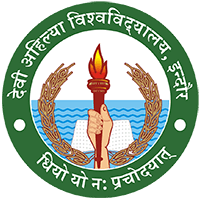
**Institute of Engineering & Technology**

**Devi Ahilya Vishwavidyalaya, Indore**

**Department of Computer Science & Engineering**



**Digital Electronics (CER3C4)**

**LAB WORK**

**(Different Types of Gates Performed on Tina Pro)**

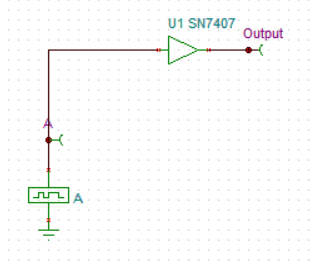
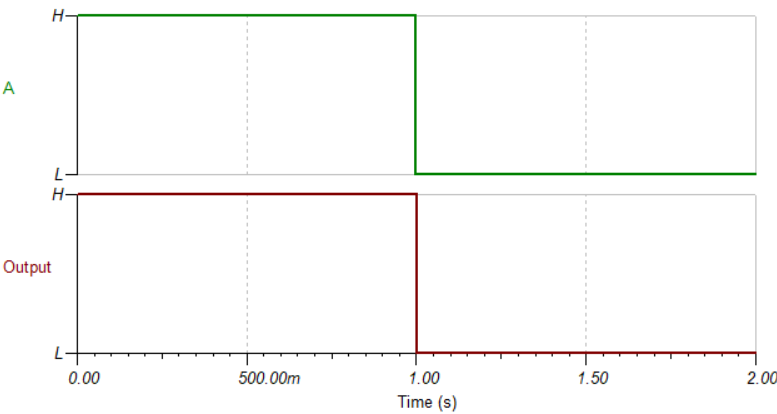
**Submitted To: Submitted By:**

**Er. Sneha Moghe Mam Tanishq Chauhan (21C3184)**

**CS-Dept CS “B” 2nd Year**

**IET-DAVV**

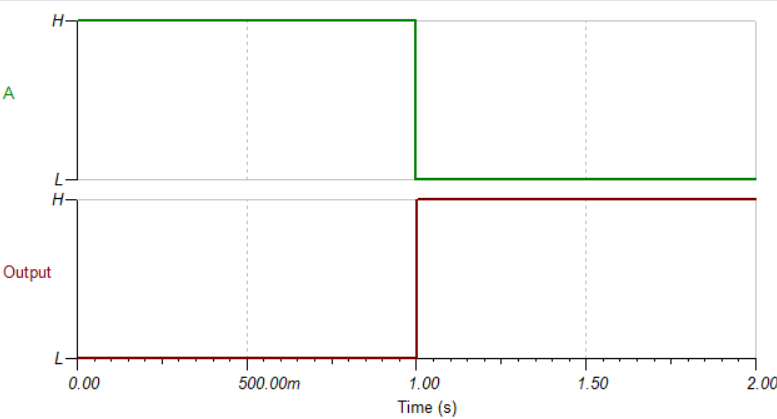
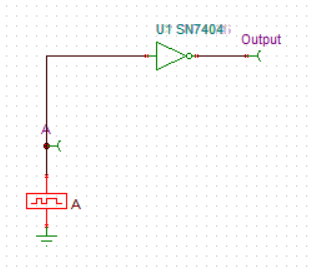
**BUFFER(1-Pin)**

****

**Truth Table**

|  |  |  |
| --- | --- | --- |
| **S.No.** | **A**  **(Input-1)** | **Output** |
| **1.** | 1 | 1 |
| **2.** | 0 | 0 |

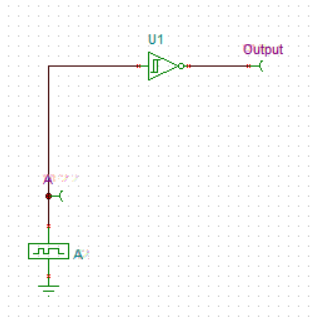
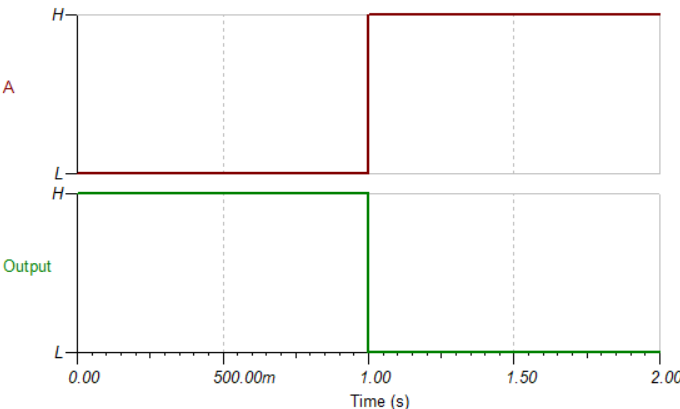
**INVERTER(1-Pin)**



**Truth Table**

|  |  |  |
| --- | --- | --- |
| **S.No.** | **A**  **(Input-1)** | **Output** |
| **1.** | 1 | 0 |
| **2.** | 0 | 1 |

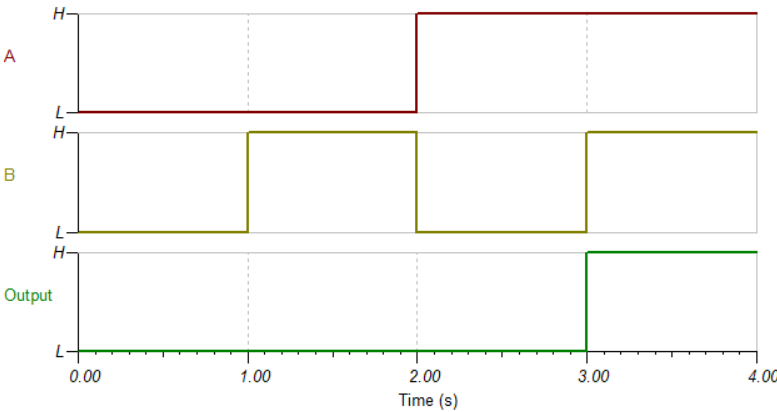
**SCHMIDT INVERTER(1-Pin)**

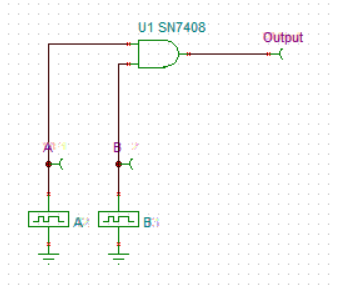
****

**Truth Table**

|  |  |  |
| --- | --- | --- |
| **S.No.** | **A**  **(Input-1)** | **Output** |
| **1.** | 0 | 1 |
| **2.** | 1 | 0 |

**AND Gate (2-Inputs)**

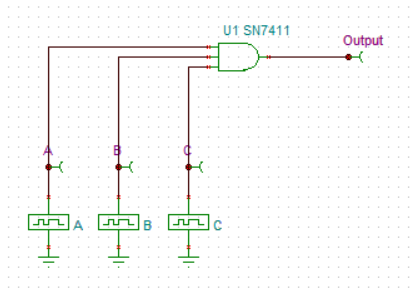
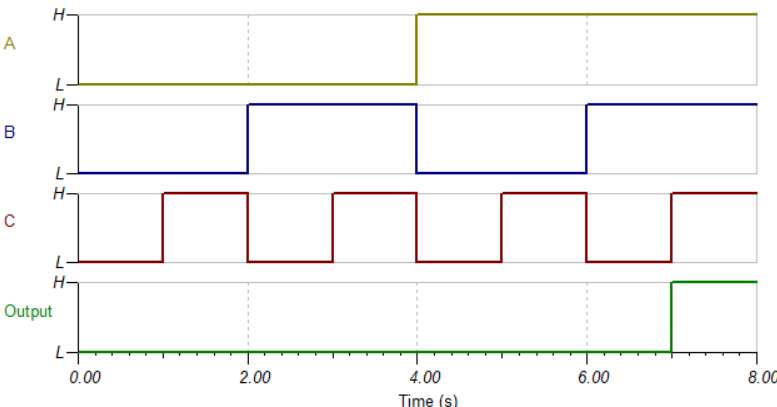
****

****

**Truth Table**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.No.** | **A**  **(Input-1)** | **B**  **(Input-2)** | **Output** |
| **1.** | 0 | 0 | 0 |
| **2.** | 0 | 1 | 0 |
| **3.** | 1 | 0 | 0 |
| **4.** | 1 | 1 | 1 |

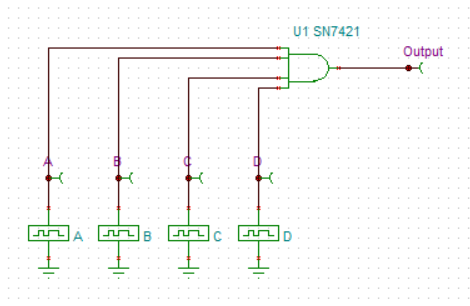
**AND Gate (3-Inputs)**

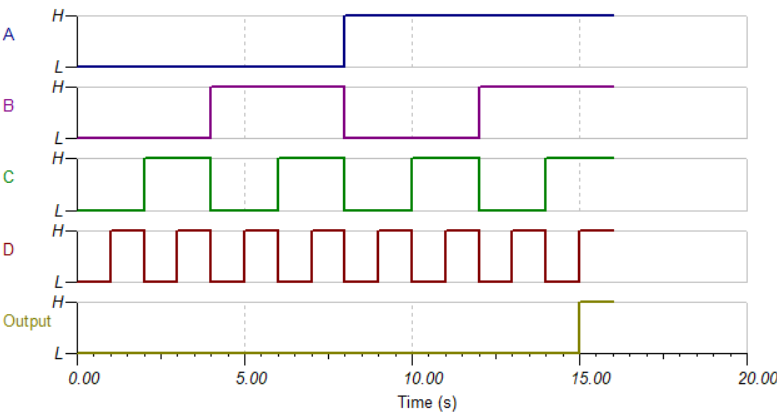
****

**Truth Table**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S.No.** | **A**  **(Input-1)** | **B**  **(Input-2)** | **C**  **(Input-3)** | **Output** |
| **1.** | 0 | 0 | 0 | 0 |
| **2.** | 0 | 0 | 1 | 0 |
| **3.** | 0 | 1 | 0 | 0 |
| **4.** | 0 | 1 | 1 | 0 |
| **5.** | 1 | 0 | 0 | 0 |
| **6.** | 1 | 0 | 1 | 0 |
| **7.** | 1 | 1 | 0 | 0 |
| **8.** | 1 | 1 | 1 | 1 |

**AND Gate (4-Inputs)**

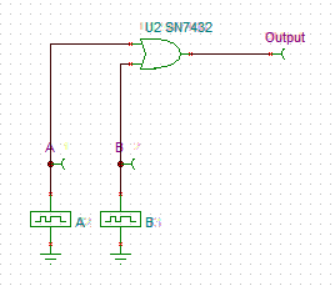
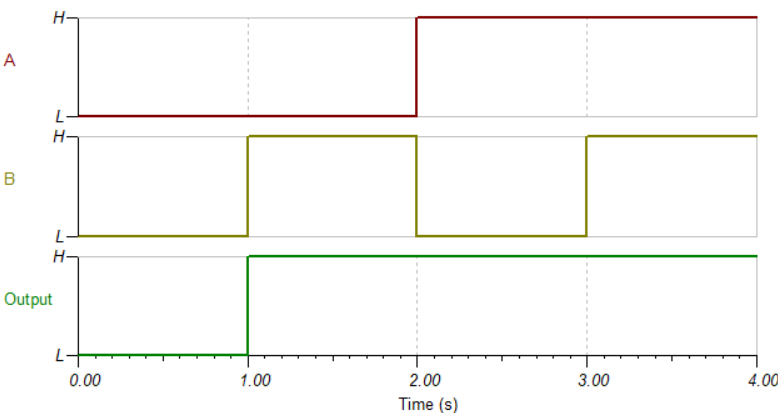




**Truth Table**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **S.No.** | **A**  **(Input-1)** | **B**  **(Input-2)** | **C**  **(Input-3)** | **D**  **(Input-4)** | **Output** |
| **1.** | 0 | 0 | 0 | 0 | 0 |
| **2.** | 0 | 0 | 0 | 1 | 0 |
| **3.** | 0 | 0 | 1 | 0 | 0 |
| **4.** | 0 | 0 | 1 | 1 | 0 |
| **5.** | 0 | 1 | 0 | 0 | 0 |
| **6.** | 0 | 1 | 0 | 1 | 0 |
| **7.** | 0 | 1 | 1 | 0 | 0 |
| **8.** | 0 | 1 | 1 | 1 | 0 |
| **9.** | 1 | 0 | 0 | 0 | 0 |
| **10.** | 1 | 0 | 0 | 1 | 0 |
| **11.** | 1 | 0 | 1 | 0 | 0 |
| **12.** | 1 | 0 | 1 | 1 | 0 |
| **13.** | 1 | 1 | 0 | 0 | 0 |
| **14.** | 1 | 1 | 0 | 1 | 0 |
| **15.** | 1 | 1 | 1 | 0 | 0 |
| **16.** | 1 | 1 | 1 | 1 | 1 |

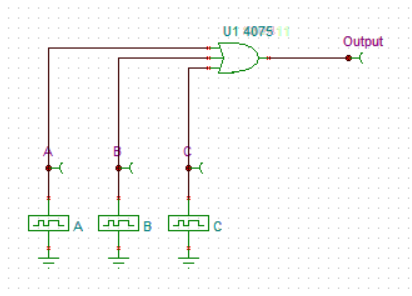
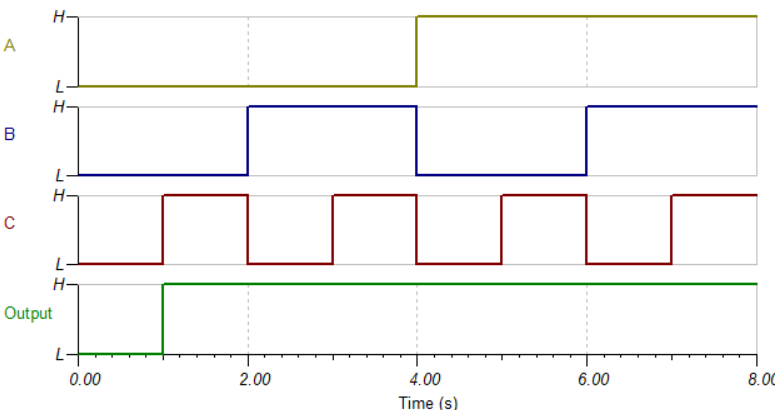
**OR Gate (2-Inputs)**

****

**Truth Table**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.No.** | **A**  **(Input-1)** | **B**  **(Input-2)** | **Output** |
| **1.** | 0 | 0 | 0 |
| **2.** | 0 | 1 | 1 |
| **3.** | 1 | 0 | 1 |
| **4.** | 1 | 1 | 1 |

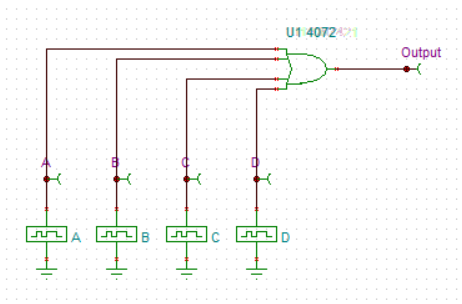
**OR Gate (3-Inputs)**

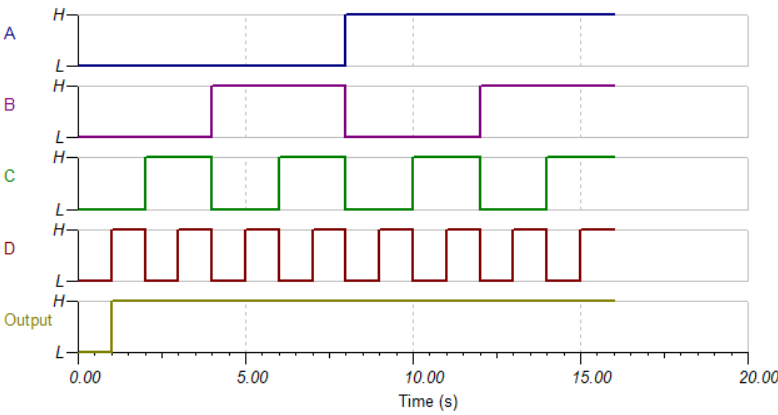
****

**Truth Table**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S.No.** | **A**  **(Input-1)** | **B**  **(Input-2)** | **C**  **(Input-3)** | **Output** |
| **1.** | 0 | 0 | 0 | 0 |
| **2.** | 0 | 0 | 1 | 1 |
| **3.** | 0 | 1 | 0 | 1 |
| **4.** | 0 | 1 | 1 | 1 |
| **5.** | 1 | 0 | 0 | 1 |
| **6.** | 1 | 0 | 1 | 1 |
| **7.** | 1 | 1 | 0 | 1 |
| **8.** | 1 | 1 | 1 | 1 |

**OR Gate (4-Inputs)**

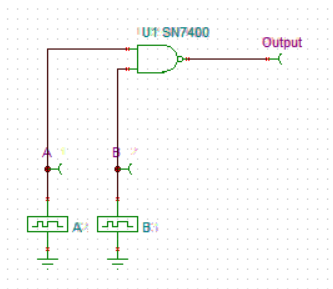
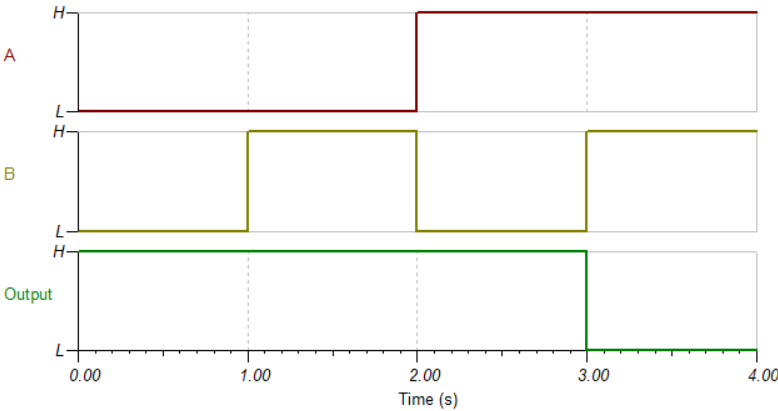
****

****

**Truth Table**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **S.No.** | **A**  **(Input-1)** | **B**  **(Input-2)** | **C**  **(Input-3)** | **D**  **(Input-4)** | **Output** |
| **1.** | 0 | 0 | 0 | 0 | 0 |
| **2.** | 0 | 0 | 0 | 1 | 1 |
| **3.** | 0 | 0 | 1 | 0 | 1 |
| **4.** | 0 | 0 | 1 | 1 | 1 |
| **5.** | 0 | 1 | 0 | 0 | 1 |
| **6.** | 0 | 1 | 0 | 1 | 1 |
| **7.** | 0 | 1 | 1 | 0 | 1 |
| **8.** | 0 | 1 | 1 | 1 | 1 |
| **9.** | 1 | 0 | 0 | 0 | 1 |
| **10.** | 1 | 0 | 0 | 1 | 1 |
| **11.** | 1 | 0 | 1 | 0 | 1 |
| **12.** | 1 | 0 | 1 | 1 | 1 |
| **13.** | 1 | 1 | 0 | 0 | 1 |
| **14.** | 1 | 1 | 0 | 1 | 1 |
| **15.** | 1 | 1 | 1 | 0 | 1 |
| **16.** | 1 | 1 | 1 | 1 | 1 |

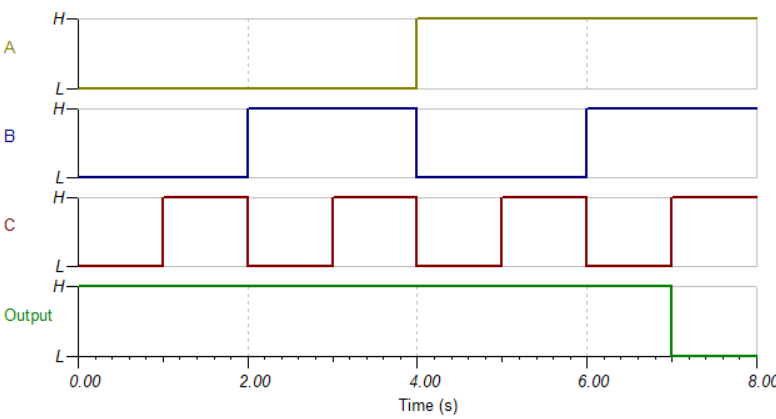
**NAND Gate (2-Inputs)**

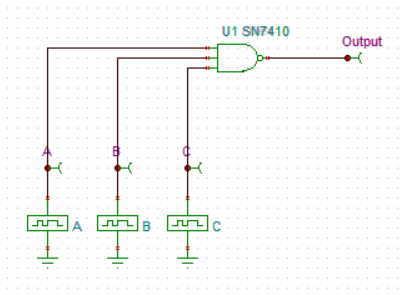
****

**Truth Table**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.No.** | **A**  **(Input-1)** | **B**  **(Input-2)** | **Output** |
| **1.** | 0 | 0 | 1 |
| **2.** | 0 | 1 | 1 |
| **3.** | 1 | 0 | 1 |
| **4.** | 1 | 1 | 0 |

**NAND Gate (3-Inputs)**

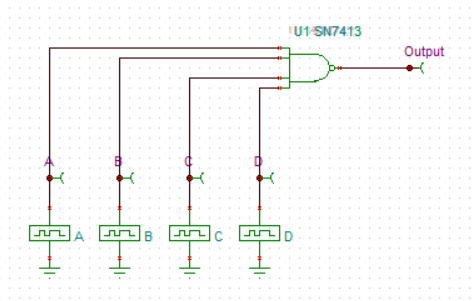
****

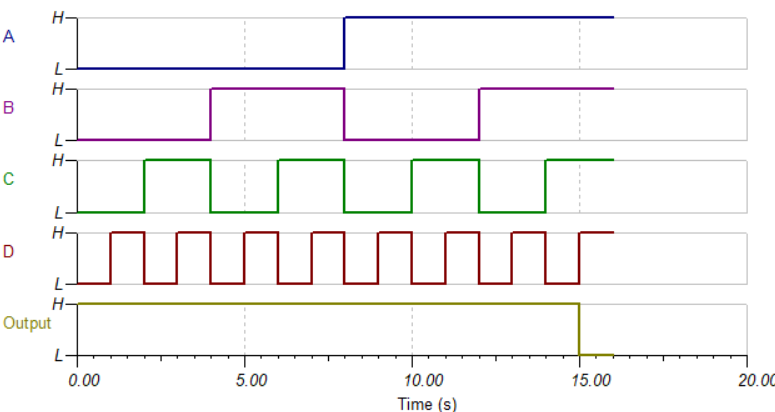
****

**Truth Table**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S.No.** | **A**  **(Input-1)** | **B**  **(Input-2)** | **C**  **(Input-3)** | **Output** |
| **1.** | 0 | 0 | 0 | 1 |
| **2.** | 0 | 0 | 1 | 1 |
| **3.** | 0 | 1 | 0 | 1 |
| **4.** | 0 | 1 | 1 | 1 |
| **5.** | 1 | 0 | 0 | 1 |
| **6.** | 1 | 0 | 1 | 1 |
| **7.** | 1 | 1 | 0 | 1 |
| **8.** | 1 | 1 | 1 | 0 |

**NAND Gate (4-Inputs)**

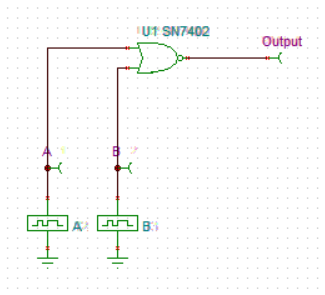
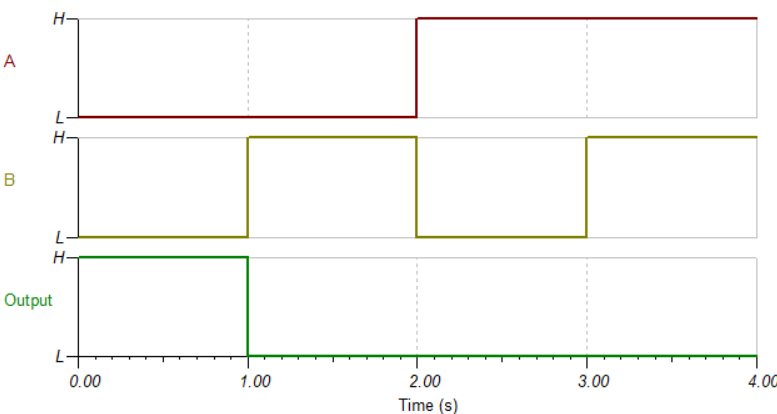




**Truth Table**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **S.No.** | **A**  **(Input-1)** | **B**  **(Input-2)** | **C**  **(Input-3)** | **D**  **(Input-4)** | **Output** |
| **1.** | 0 | 0 | 0 | 0 | 1 |
| **2.** | 0 | 0 | 0 | 1 | 1 |
| **3.** | 0 | 0 | 1 | 0 | 1 |
| **4.** | 0 | 0 | 1 | 1 | 1 |
| **5.** | 0 | 1 | 0 | 0 | 1 |
| **6.** | 0 | 1 | 0 | 1 | 1 |
| **7.** | 0 | 1 | 1 | 0 | 1 |
| **8.** | 0 | 1 | 1 | 1 | 1 |
| **9.** | 1 | 0 | 0 | 0 | 1 |
| **10.** | 1 | 0 | 0 | 1 | 1 |
| **11.** | 1 | 0 | 1 | 0 | 1 |
| **12.** | 1 | 0 | 1 | 1 | 1 |
| **13.** | 1 | 1 | 0 | 0 | 1 |
| **14.** | 1 | 1 | 0 | 1 | 1 |
| **15.** | 1 | 1 | 1 | 0 | 1 |
| **16.** | 1 | 1 | 1 | 1 | 0 |

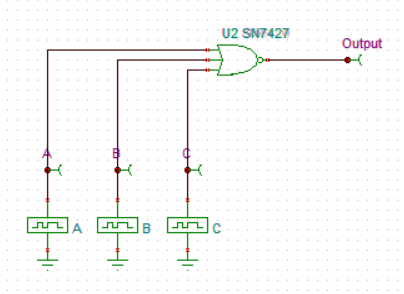
**NOR Gate (2-Inputs)**

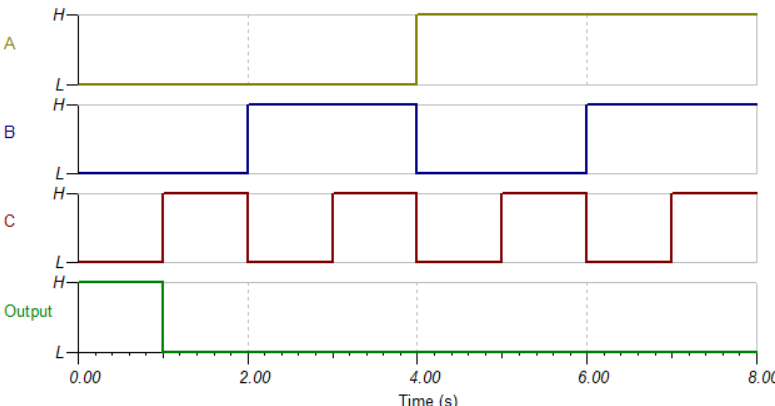
****

**Truth Table**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.No.** | **A**  **(Input-1)** | **B**  **(Input-2)** | **Output** |
| **1.** | 0 | 0 | 1 |
| **2.** | 0 | 1 | 0 |
| **3.** | 1 | 0 | 0 |
| **4.** | 1 | 1 | 0 |

**NOR Gate (3-Inputs)**

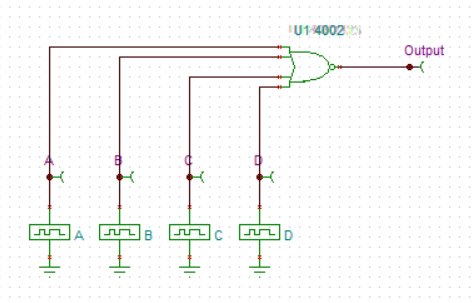
****

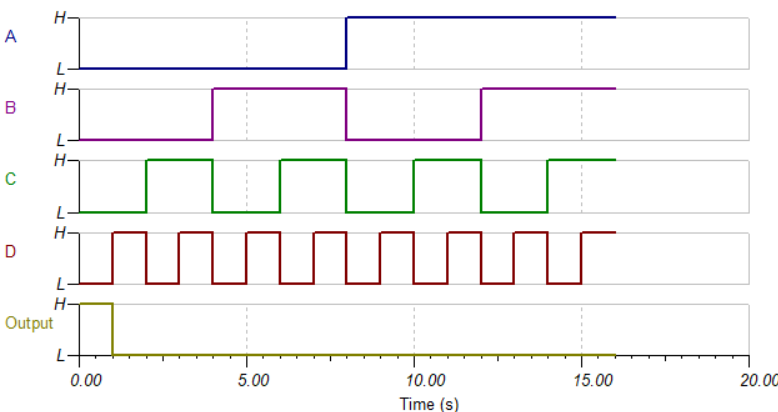
****

**Truth Table**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S.No.** | **A**  **(Input-1)** | **B**  **(Input-2)** | **C**  **(Input-3)** | **Output** |
| **1.** | 0 | 0 | 0 | 1 |
| **2.** | 0 | 0 | 1 | 0 |
| **3.** | 0 | 1 | 0 | 0 |
| **4.** | 0 | 1 | 1 | 0 |
| **5.** | 1 | 0 | 0 | 0 |
| **6.** | 1 | 0 | 1 | 0 |
| **7.** | 1 | 1 | 0 | 0 |
| **8.** | 1 | 1 | 1 | 0 |

**NOR Gate (4-Inputs)**

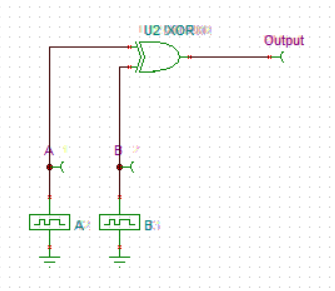
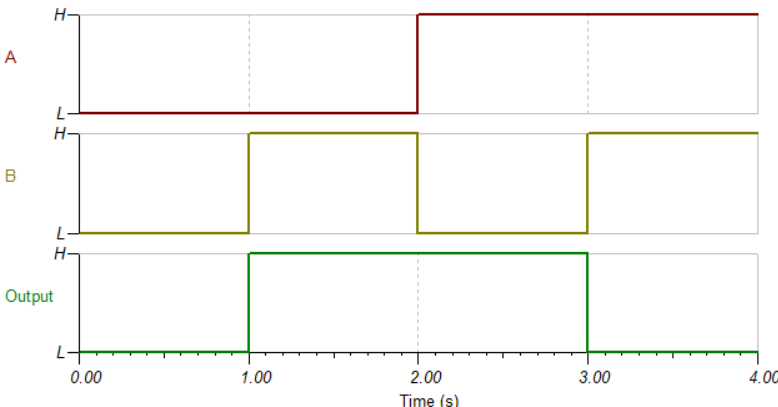
****

****

**Truth Table**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **S.No.** | **A**  **(Input-1)** | **B**  **(Input-2)** | **C**  **(Input-3)** | **D**  **(Input-4)** | **Output** |
| **1.** | 0 | 0 | 0 | 0 | 1 |
| **2.** | 0 | 0 | 0 | 1 | 0 |
| **3.** | 0 | 0 | 1 | 0 | 0 |
| **4.** | 0 | 0 | 1 | 1 | 0 |
| **5.** | 0 | 1 | 0 | 0 | 0 |
| **6.** | 0 | 1 | 0 | 1 | 0 |
| **7.** | 0 | 1 | 1 | 0 | 0 |
| **8.** | 0 | 1 | 1 | 1 | 0 |
| **9.** | 1 | 0 | 0 | 0 | 0 |
| **10.** | 1 | 0 | 0 | 1 | 0 |
| **11.** | 1 | 0 | 1 | 0 | 0 |
| **12.** | 1 | 0 | 1 | 1 | 0 |
| **13.** | 1 | 1 | 0 | 0 | 0 |
| **14.** | 1 | 1 | 0 | 1 | 0 |
| **15.** | 1 | 1 | 1 | 0 | 0 |
| **16.** | 1 | 1 | 1 | 1 | 0 |

**EX-OR Gate (2-Inputs)**

****

**Truth Table**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.No.** | **A**  **(Input-1)** | **B**  **(Input-2)** | **Output** |
| **1.** | 0 | 0 | 0 |
| **2.** | 0 | 1 | 1 |
| **3.** | 1 | 0 | 1 |
| **4.** | 1 | 1 | 0 |